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An Explicit Crosstalk Aware Delay Modelling For On-Chip RLC Interconnect for Ramp Input with Skin Effect

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Abstract-

With the increase in frequency towards the giga hertz range, the analysis of high frequency effects like skin effect etc. are becoming extensively predominant and important for high speed VLSI design. Skin effect attenuates the high frequency components of a signal more than that of the low frequency components. Noise produced in any interconnect segment may degrade the performance of the entire system. Hence accurate noise and delay modelling for RLC lines is critical for timing and system integrity analysis. Skin effect alters the values of the resistance and also the inductance, which in turn affects the system integrity in particular and its response as a whole. Till now the skin effect has been neglected for modelling the on-chip interconnects. But at high frequencies of the order of gigahertz the skin effect becomes dominant factor and needs to be considered for accurate performance analysis. In this paper, we have proposed an accurate modelling of crosstalk voltage and delay response including skin effect for ramp input in on-chip VLSI RLC interconnect. The voltage response at the output node is analysed. From the response, the crosstalk noise and delay is estimated analytically for the on-chip RLC interconnect. This paper also addresses a novel analytical model to find the impact of skin effect on the noise and delay variation in RLC interconnect, without considering the skin effect modelling in inductance under ramp input. In the proposed work the resistance variation due to the skin effect is considered in a two wire transmission line model. The correlation between the skin effect and noise is also considered.

Keywords- VLSI , RLC line, Interconnects, Crosstalk, Noise, Delay

I. INTRODUCTION

Since late 80's, there have been a number of significant researches towards better and accurate modelling and characterization of the resistance, capacitance and the inductance of on-chip VLSI interconnect. In recent years, increase in bandwidth requirements have led to the research into low-loss on-chip interconnects, which theoretically can achieve very high bandwidth [1]. For integrated circuits in the deep submicron (DSM) technology, interconnects play an important role in determining the chip performance and signal integrity. In deep submicron design, interconnect delay is shown to be ten to few hundred times larger than the intrinsic gate delay [2]. In order to reduce interconnect delay, wire-sizing is found to be an effective way. On-chip interconnect analysis begins with an in-depth coverage of delay metrics, including the ubiquitous Elmore delay [3] and its many variations. The study and analysis of interconnect line has become very important issue because as integrated circuit feature sizes continue to scale well below 0.18µm, active device counts are reaching hundreds of millions [4]. The amount of interconnects among the devices tends to grow super linearly with the transistor counts, and the chip area is often limited by the physical interconnect area. Due to these interconnect area limitation, the interconnect dimensions are scaled with the devices whenever possible. Wire sizing [5] is found to be effective in reducing interconnect delays. Continuous wire sizing is a well suited approach which describes the wire by a continuous shape function. Studies on Elmore delay model have found that optimal shape function is exponential or near exponential. As frequency increases, current density within the conductor varies in such a way that it tends to exclude magnetic flux inside the conductor. This situation results in an apparent increase in resistance of the conductor because maximum current is concentrated near the surface and edges of the conductor, and it also causes the effective inductance of the conductor to decrease as frequency increases. These two effects become especially important when modelling the performance of high-speed data signals. Accurate prediction of propagation delay, crosstalk and pulse distortion in high-speed interconnects is strongly dependent on the per-unit parameter's model accuracy. As the technology has started working on the high frequencies high frequency effect like skin effect and proximity effects has become significant. The reason behind the importance of considering such effect is that, these effects affects the system integrity at large scale.

II. BASIC THEORY

This is a well know fact that propagation delay increases with the skin effect in an on-chip interconnect. Skin effect will also affect the optimality of the system. The skin effect can be represented at the circuit level as a combination of frequency dependent resistance and inductance. However, frequency dependent circuit elements are not suitable for time-domain analysis, therefore a circuit representation based on frequency independent elements is desirable [6]. When a transmission line model is necessary, either a Spice-compatible distributed RLC model is used or else a full transmission line model is needed. Which is chosen depends on the accuracy needed and also the capability of an available circuit simulation program[7]. A range of models are used for interconnects depending on:

1) The accuracy required nets carrying analog signals need to be modelled more
2) The amenability of the net to modelling.
3) The frequency of operation.

Short on-chip interconnects are commonly modelled as RLC networks where the inductor and capacitor networks are arrived at separately using static calculations of the effect of very small segments of interconnect on other small segments. Uniform interconnects (with regular cross-section) can be modelled by determining the characteristics of the transmission line, e.g. ZO and y versus frequency, or arriving at a distributed lumped element circuit.[7].Since the frequency dependent behaviour is easy to compute and observe, in any circuit ,consisting of frequency dependent components skin effect modelling can be performed.

Intuitively, to mimic the skin effect, a conductor can be thought of as made up of concentric shells. At low frequencies, all the shells are carrying currents, minimizing the resistance and maximizing the internal inductance. As frequency increases, due to the magnetic field inside the conductors, the inner most shells gradually turn off and only the outer shells stay active, thus increasing the resistance and decreasing the internal inductance. This can also be achieved by parallel combination of impedance branches, where each branch will have a resistance and inductance in series as shown in the figure (1): [8]

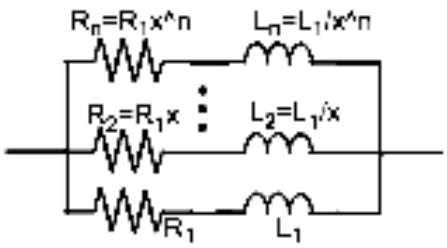


Figure (1)

The "Skin Effect" is the tendency of high frequency current to concentrate near the outer edge, or surface, of a conductor, instead of flowing uniformly over the entire cross sectional area of the conductor. The higher the frequency, the greater the tendency for this effect to occur. There are three possible reasons we might care about skin effect. The resistance of a conductor is inversely proportional to the cross sectional area of the conductor. If the cross sectional area decreases, the resistance goes up. The skin effect causes the effective cross sectional area to decrease. Therefore, the skin effect causes the effective resistance of the conductor to increase. The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become a function of frequency (instead of being constant for all frequencies.) This, in turn, impacts the impedance of the conductor. If we are concerned about controlled impedance traces and transmission line considerations, the skin effect causes trace termination techniques to become much more complicated. If the skin effect causes the effective cross sectional area of a trace to decrease and its resistance to increase, then the trace will heat faster and to a higher temperature at higher frequencies for the same level of current [9]. There are a number of approaches available where the on-chip interconnect is modelled as distributed RLC segments for accurate performance parameters modelling [10-14]. But these models do not consider the high frequency skin effect phenomena.

III. CROSS TALK

Crosstalk is defined as the energy imparted to a transmission line due to signals in adjacent lines. Crosstalk magnitude is a function of rise time, signal line geometry and net configuration (type of terminations, etc.). A common method of shielding is to place ground or power lines at the sides of a victim signal line to reduce noise and delay uncertainty [15]. The crosstalk between two coupled interconnects is often neglected when a shield is inserted, significantly underestimating the coupling noise. The crosstalk noise between two shielded interconnects can produce a peak noise of 15% of VDD in a 0.18 µm CMOS technology [16]. An accurate estimate of the peak noise for shielded interconnects is therefore necessary. In the complicated multilayered interconnect system, signal coupling and delay strongly affect circuit performances. Thus, accurate interconnect characterization and modelling are essential for today's VLSI circuit design. Two major impacts of cross talk are: (1) cross talk induced delays, which change the signal propagation time, and thus may lead to setup or hold time failures; (2) cross talk glitches, which may cause voltage spikes on wire, resulting in false logic behaviour. Crosstalk affects mutual inductance as well as inter-wire capacitance. When the connectors in high speed digital designs are considered, the mutual inductance plays a predominant role compared to the inter-wire capacitance. The effect of mutual inductance is significant in deep submicron technology (DSM) technology since the spacing between two adjacent bus lines is very small. The mutual inductance induces a current from the aggressor line onto a victim line which causes crosstalk between the

parallel lines. Which in turn alters the performance parameters of on-chip VLSI interconnect system.

In multi-conductor systems, crosstalk can cause two detrimental effects: first, crosstalk will change the performance of the transmission lines in a bus by modifying the effective characteristic impedance and propagation velocity. Secondly, crosstalk will induce noise onto other lines, which may further degrade the signal integrity and reduce noise margins.[17]

IV. PROPOSED WORK

The proposed work is divided in two sub-sections. In the first sub-section, a novel analytical crosstalk model of RLC interconnect is proposed which does not included the skin effect; whereas, in the second sub-section, the skin effect is considered for interconnect modelling through simulation of the proposed RLC model. Note that the skin effect makes an adverse effect on the resistance and the inductance. However, this paper only considered the skin effect onto the resistance. The resistance increases with the skin effect; whereas, a decrease in the inductance is accounted.

A. Crosstalk Modelling of RLC Interconnect Analysis Without Skin Effect

In this section a new analytical model of RLC interconnects is proposed. This analysis considers the following interconnect coupling circuit:

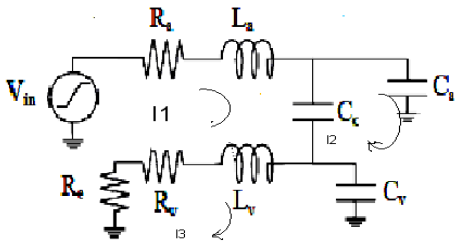


Figure 2: Analytical Model of RLC interconnect

Now applying the simple loop analysis, the following equations are obtained in terms of RLC:

For first loop:

$$V_{in}(t) = I_1(t).R_a + L_a.\left(\frac{d}{dt}I_1(t)\right) + \frac{1}{C_c}[I_1(t) - I_2(t)] \quad (5)$$

For second loop:

$$\frac{1}{C_c}[I_2(t) - I_1(t)] - \frac{1}{C_a}I_2(t) = 0 \quad (6)$$

For third loop:

$$R_e I_3(t) + R_v \cdot I_3(t) + L_v \cdot \frac{d}{dt}(I_3(t)) + \frac{1}{C_c} \cdot I_3(t) = 0 \quad (7)$$

Taking Laplace Transform of (5)- (7), the following equations are obtained:

$$V_{in}(s) = I_1(s)R_a + sL_aI_1(s) + \frac{[I_1(s) - I_2(s)]}{sC_c} \quad (8)$$

$$\frac{1}{sC_c}[I_2(s) - I_1(s)] - \frac{1}{sC_a}I_2(s) = 0 \quad (9)$$

$$R_eL_3(s) + R_vI_3(s) + sL_vI_3(s) + \frac{1}{sC_v}.I_3(s) = 0 \quad (10)$$

From (9), the following can be derived:

$$\left[\frac{1}{sC_c} - \frac{1}{sC_a}\right]I_2(s) = \frac{1}{sC_c}I_1(s) \quad (11)$$

Or (12)

$$I_2(s) = \frac{I_1(s)}{sC_c\left(\frac{1}{sC_c} - \frac{1}{sC_a}\right)}$$

So, $I_2(s) = I_1(s)\left(\frac{C_a}{C_a - C_c}\right)$ (13)

From equation (8),

$$V_{in}(s) = I_1(s).R_a + sL_aI_1(s) + \frac{1}{C_c}I_1(s) - \frac{1}{C_c}I_1(s).\frac{C_a}{C_a - C_c} \quad (14)$$

Or, (15)

$$V_{in}(s) = I_1(s)\left[R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)\right]$$

So, (16)

$$I_1(s) = \frac{V_{in}(s)}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)}$$

With the simple loop analysis it can be found that

$$I_3 = |I_1 - I_2| \quad (17)$$

Therefore, using I_1 and I_2, the third current can be derived which is given as,

$$I_3(s) = \frac{V_{in}(s)C_c}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)(C_a - C_c)} \quad (18)$$

Applying the current divider rule, the current in the victim line capacitor may be found. This finally yields to,

$$I_x = I_3\frac{R_2}{R_1 + R_2} \quad (19)$$

Where $R_1 = (R_e + R_v + sL_v) or, R_2 = \frac{1}{sC_v}$

$$I_x = \frac{V_{in}(s)C_c}{R_a + sL_a + \frac{1}{C_c}\left(1 - \frac{C_a}{C_a - C_c}\right)(C_a - C_c)} \times \frac{R_e + R_v + sL_v}{R_e + R_v + sL_v + \frac{1}{sC_v}} \quad (20)$$

The output voltage is given as,

$$V_{co}(s) = I_x \times \frac{1}{sC_v} \quad (21)$$

From (20) and (21) we have,

$$V_{co}(s)=\frac{V_{in}(s)}{sC_v}\left[\frac{C_c(R_e+R_v+sL_v)}{\left(R_a+sL_a+\frac{1}{C_c\left(1-\frac{C_a}{C_a-C_c}\right)}\right)\times\left(R_e+R_v+s\left(L_v+\frac{1}{s^2C_v}\right)\right)\times(C_a-C_c)}\right] \quad (22)$$

Some important assumptions that have been made in this paper are as follows:

$$R_e+R_v=A$$
$$R_a+\frac{1}{C_c}\left[1-\frac{C_a}{C_a-C_c}\right]=B \quad (23)$$

For ramp input, $V_{in}=\frac{V_0}{s^2}$ (24)

Using the above assumptions and applying partial fraction theory yields,

$$V_{co}(s)=\frac{V_0}{s^3(C_a-C_c)}\left[\frac{C_c(A+sL_v)}{(B+sL_a)\times(1+A+sL_v)}\right] \quad (25)$$

$$S(s)=\frac{F_1}{s}+\frac{F_2}{s^2}+\frac{F_3}{s^3}\frac{F_4}{(B+sL_a)}+\frac{F_5}{(1+A+sL_v)} \quad (26)$$

$$F_3=(S(s).s^3)|_{s=0}=\left[\frac{C_c(A+sL_v)}{(B+sL_a)(1+A+sL_v)}\right]|_{s=0} \quad (27)$$

$$=\frac{C_c.A}{[B(A+1)]}$$

$$F_1=-(F_4.L_v+F_5.L_a)$$

$$=\left(\frac{C_c\left(A-\frac{B}{L_a}.L_v\right).L_v}{\left((A+1)-\frac{B}{L_a}.L_a\right)\left(-\frac{B}{L_a}\right)^3}+\frac{C_c.L_a}{\left(B-(A+1).\frac{L_a}{L_v}\right).\left(\frac{1+A}{L_v}\right)^3}\right) \quad (28)$$

$$F_2(B+AB)+F_3(B.L_v+L_a+A.L_a)=C_c.L_v$$

$$F_2=\left(\frac{C_c.L_v-F_3(B.L_v+L_a+A.L_a)}{(B+A.B)}\right) \quad (29)$$

$$=\frac{C_c.L_v}{B.(1+A)}-\frac{C_c.A.(B.L_v+L_a+AL_a)}{[(1+A).B]^2}$$

$$F_4=S(s)(B+sL_a)|_{s=-\frac{B}{L_a}}=\frac{C_c(A+sL_v)}{(1+A+sL_v)s^2}|_{s=-\frac{B}{L_a}} \quad (30)$$

$$F_5=S(s)(1+A+sL_v)|_{s=-\frac{A+1}{L_v}}$$

$$=\frac{C_c\left(A-\frac{B}{L_a}L_v\right)}{\left[(A+1)-\frac{B}{L_a}L_v\right]\left(-\frac{B}{L_a}\right)^3} \quad (31)$$

$$=\frac{C_c(A+sL_v)}{s^2(B+sL_a)}|_{s=-\frac{(A+1)}{L_v}}$$

$$=-\frac{C_c}{\left[B-(A+1)\frac{L_a}{L_v}\right]\left(\frac{1+A}{L_v}\right)^3}$$

Taking the Laplace inverse transform of (25) and with the help of (26)-(31), one can derive the explicit expression for $V_{co}(t)$ and it is given in (32).

$$V_{co}(t)=\frac{V_0}{(C_a-C_c)}(\alpha_1+\beta_1+\chi_1+\kappa_1+\zeta_1) \quad (32)$$

where

$$\alpha_1=\left(\frac{C_c\left(A-\frac{B}{L_a}.L_v\right).L_v}{\left[A+1-\frac{B}{L_a}.L_v\right]\cdot\left[-\frac{B}{L_a}\right]^3}+\frac{C_c.L_a}{\left[B-(A+1).\frac{L_a}{L_v}\right]\cdot\left[\frac{1+A}{L_v}\right]^3}\right)u(t)$$

$$\beta_1=\left[\frac{C_c.L_v}{B.(A+1)}-\frac{C_c.A(B.L_v+L_a+A.L_a)}{[(1+A).B]^2}\right]t.u(t)$$

$$\chi_1=\frac{1}{2}\left[\frac{C_c.A}{(1+A).B}.t^2\right].u(t)$$

$$\kappa_1=\frac{C_c\left(A-\frac{B}{L_a}L_v\right)}{\left[(A+1)-\frac{B}{L_a}L_v\right]\left(-\frac{B}{L_a}\right)^3}e^{-\frac{B}{L_a}t}$$

$$\zeta_1=-\frac{C_c}{\left[B-(1+A)\frac{L_a}{L_v}\right]\left[\frac{A+1}{L_v}\right]^3}e^{-\frac{(1+A)}{L_v}t}$$

The equation (32) describes the coupling noise voltage without the presence of skin effect phenomena.

Crosstalk Modelling of RLC Interconnect With Skin Effect

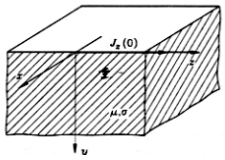
In this section, we have considered the performance variations of interconnect due to the presence of the skin effect phenomena. The skin effect is the tendency of high frequency current density to be highest at the surface of a conductor and then to decay exponentially towards the centre [18].

The possible reasons for which one must care the skin effect are the following:

The resistance of a conductor is inversely proportional to the cross sectional area of the conductor. If the cross sectional area decreases, the resistance goes up. The skin effect causes the effective cross sectional area to decrease. Therefore, the

skin effect causes the effective resistance of the conductor to increase [19].

The skin effect is a function of frequency. Therefore, the skin effect causes the resistance of a conductor to become the function of frequency. This, in turn, affects the impedance of the conductor. The inductance decreases as the frequency increases [19]. It is simple to analyze the skin effect in a homogeneous conducting half space with the current parallel to the interface. Let the current is in z-direction and y axis is normal to the interface as shown in the Figure 2.



Homogeneous conducting half space

If the angular frequency of the current is ω, and the medium has a conductivity σ, and permeability μ, the complex current density is found to be:

$$J_z(y) = J_z(0).e^{-ky}e^{-jky}$$

where, $$k = \sqrt{\frac{\omega\sigma\mu}{2}}$$

The intensity of the current density vector decrease exponentially with increasing y. At a distance δ,

$$\delta = \frac{1}{k} = \sqrt{\frac{2}{\omega\mu\sigma}} \quad (33)$$

The amplitude of the current density vector decreases 1/e of its value $J_z(0)$ at the boundary surface. This distance is known as the "skin depth". In Table-1, the skin depths of various materials are shown.

Skin depth for Copper is $\sigma = 57\times10^6 S/m, \mu = \mu_0$ for iron $\sigma = 10^7 S/m, \mu_r = 1000$, for sea water $\sigma = 4S/m, \mu = \mu_0$, for wet soil $\sigma = 0.01S/m, \mu = \mu_0$.

TABLE I. SKIN DEPTH FOR VARIOUS MATERIALS

Material	f= 60Hz	f = 10^3 Hz	f = 10^6 Hz	f=10^9 Hz
Copper	8.61 mm	2.1m	.067 mm	2.11 μm
Iron	0.65 mm	0.16 mm	5.03μ m	0.01 6μm
Sea Water	32.5 m	7.96 m	.25m	7.96 μm
Wet Soil	650 m	159m	5.03 m	0.16 μm

It is mentioned earlier that we have only considered the skin effect on resistance. So for calculating the total effect on the impedance we have to calculate the output impedance.

From the Figure 1,

$$Z_1 = \frac{[R_v + R_e + sL_v]\times\frac{1}{sC_v}}{(R_v + R_e + sL_v) + \frac{1}{sC_v}} \quad (34)$$

$$Z_2 = \frac{(R_v + R_e + sL_v)\times\frac{1}{sC_v}}{(R_v + R_e + sL_v)} + \frac{1}{sC_c} \quad (35)$$

$$Z_3 = \left\{\frac{\left[\frac{[R_v + R_e + sL_v]\times\frac{1}{sC_v}}{\left[R_v + R_e + sL_v + \frac{1}{sC_v}\right]} + \frac{1}{sC_c}\right]\times\frac{1}{sC_a}}{\frac{(R+R+sL)\times\frac{1}{sC}}{(R_v + R_e + sL_v) + \frac{1}{sC_v}} + \frac{1}{sC_c} + \frac{1}{sC_a}}\right\} \quad (36)$$

The total output resistance in RLC interconnects is given in (37)

$$Z_0 = \left[\frac{\left(\frac{(R+R+sL)\times\frac{1}{sC_v}}{(R_v + R_e + sL_v) + \frac{1}{sC_v}}\right)\times\frac{1}{sC_a}}{(R_v + R_e + sL_v)\times\frac{1}{sC_v} + \frac{1}{sC_c} + \frac{1}{sC_a}}\right] + (R_a + sL_a) \quad (37)$$

Skin effect on resistance can be calculated by using the following equations:

$$R_{total} = R_{DC} + \sqrt{f}\,R_{AC}, \quad (38)$$

Where, $$R_{DC} = \frac{\rho L}{W.t} \quad (39)$$

$$R_{AC} = \frac{\rho L}{A_{current\_densityar\_area}} = \frac{L\rho}{\omega\sqrt{\frac{2}{\omega\sigma\mu}}} = \frac{L\sqrt{\rho}}{\omega\sqrt{2}}\sqrt{\mu f} \quad (40)$$

Therefore,

$$R = R_{total} = \frac{\rho L}{Wt} + \frac{L\sqrt{\rho}}{\omega\sqrt{2}}.\sqrt{\mu f} \quad (41)$$

It is evident from the above equation that resistance increases as a function of the square root of the frequency due to the skin effect.

B. Cross Talk Voltage and delay with Skin Effect

Thus equation (32) can be used to find the closed form expression of the cross talk noise with skin effect.

$$V_{co}(t) = \frac{V_0}{(C_a - C_c)}\left(\alpha_2 + \beta_2.t + \chi_2.t^2 + \kappa_2.e^{-\frac{B_{skin}}{L_a}t} + \zeta_2.e^{-\frac{(1+A_{skin})}{L_v}t}\right) \quad (42)$$

Where,

$$\alpha_2 = \left(\frac{C_c\left(A_{skin} - \frac{B_{skin}}{L_a}.L_v\right).L_v}{\left[A_{skin}+1-\frac{B_{skin}}{L_a}.L_v\right]\cdot\left[-\frac{B_{skin}}{L_a}\right]^3} + \frac{C_c.L_a}{\left[B_{skin}-(A_{skin}+1).\frac{L_a}{L_v}\right]\cdot\left[\frac{1+A_{skin}}{L_v}\right]^3} \right) u(t)$$

$$\beta_2 = \left[\frac{C_c.L_v}{B_{skin}.(A_{skin}+1)} - \frac{C_c.A_{skin}(B_{skin}.L_v + L_a + A_{skin}L_a)}{[(1+A_{skin}).B_{skin}]^2} \right].u(t)$$

$$\chi_2 = \frac{1}{2}\left[\frac{C_c.A_{skin}}{(1+A_{skin}).B_{skin}}\right].u(t)$$

$$\kappa_2 = \frac{C_c\left(A_{skin} - \frac{B_{skin}}{L_a}L_v\right)}{\left[(A_{skin}+1) - \frac{B_{skin}}{L_a}L_v\right]\left(-\frac{B_{skin}}{L_a}\right)^3}$$

$$\zeta_2 = -\frac{C_c}{\left[B_{skin}-(1+A_{skin})\frac{L_a}{L_v}\right]\left[\frac{A_{skin}+1}{L_v}\right]^3}$$

Delay:-

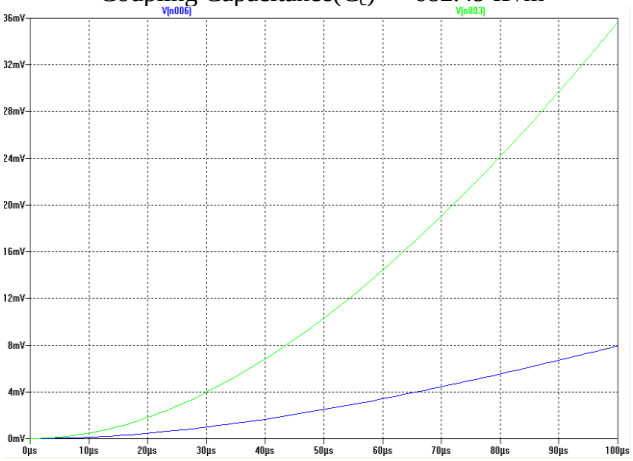
$$t = \frac{0.5(C_a - C_c) + \alpha_2 - (\kappa_2 + \xi_2)}{\beta_2 - (\kappa_2.m + \xi_2.n)} \qquad (43)$$

V. SIMULATION RESULTS AND DISCUSSIONS

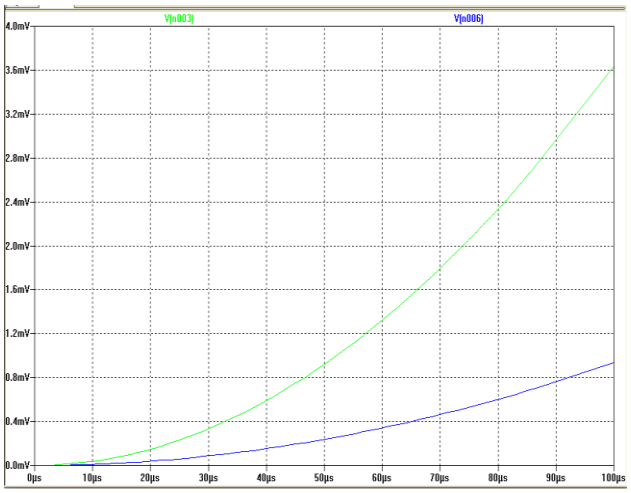
The motive of this paper is to make a reflection on the skin effect's impact on the on-chip interconnect and its performance under ramp input. It can be analyzed by the simulation result that the delay has been increased. This is due to the fact that skin effect has an adverse effect on the resistance, so with the existence of the skin effect the resistance is increased as discussed in the section B. This increase in the resistance in turn increases the delay which is undesirable in terms of speed of the chip. The configuration of circuit for simulation is shown in Figure.4. We now develop a simple model for distributed RLC interconnect line. The high-speed interconnect system consist of two coupled interconnect lines and ground and the length of the lines is d =100 um. These lines are excited by the voltage source of 1.8 V with driver resistance of R_s. The extracted values for the parameters R, L, and C are given in Table II [20]. We have obtained cross talk noise voltage from SPICE with proposed model in both the cases i.e. with and without considering the skin effect on the interconnect lines. Figure (3) and (4) demonstrate the behaviour of output node crosstalk noise voltage curve with and without considering the skin effect respectively.

TABLE II. RLC PARAMETERS FOR A MINIMUM- SIZED WIRES IN A 0.18µM TECHNOLOGY.

Parameter(s)	Value/m
Resistance(R)	120 kΩ/m
Inductance(L)	270 nH/m
Capacitance(C)	240 pF/m
Coupling Capacitance(C_c)	682.49 fF/m



Fig(3) Delay obtained without skin effect under ramp input



Figure(4) delay obtained with skin effect under ramp input

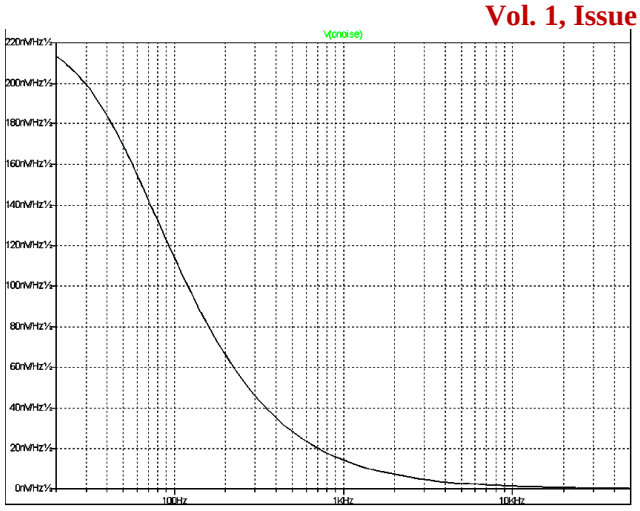
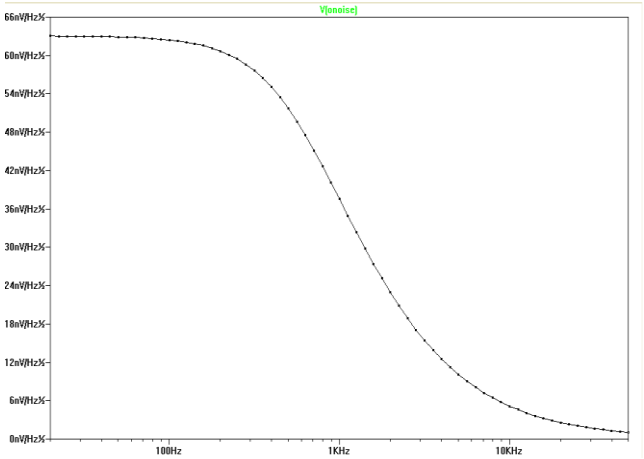


Figure (3) : Output node noise with considering skin effect



Figure(4): Output node noise without considering skin efffect

TABLE III. EXPERIMENTAL RESULT UNDER RAMP INPUT WITHOUT SKIN EFFECT

Ex	R_s (KΩ)	C_L (fF)	SPICE Delay (ms)	Proposed Model Delay (ms)
1	1	10	0.1123	0.1152
2	5	50	0.1198	0.1171
3	10	750	0.1479	0.1474
4	50	1000	0.1779	0.1881
5	100	1500	0.1995	0.1994

TABLE IV. EXPERIMENTAL RESULT UNDER RAMP INPUT WITH SKIN EFFECT

Ex	R_s (KΩ)	C_L (fF)	SPICE Delay (ms)	Proposed Model Delay (ms)
1	1	10	0.1739	0.1921
2	5	50	0.358	0.6437
3	10	750	0.7739	0.8129
4	50	1000	0.8475	0.8942
5	100	1500	0.9757	0.9976

We compare the delays obtained from SPICE with those proposed model in both the cases i.e. with and without considering the skin effect on the interconnect lines. Table 3 and Table 4 compare the delay obtained from SPICE with those found using the proposed model without and with considering skin effect. Note that the difference between the proposed model and the SPICE delay is about 2% in both the cases.

The simulation shows that failure to account for the skin effect leads to three different errors. First, since the internal inductance is included in the line parameters, the line delay is overestimated. This error could be removed by including only the external inductance in the RLC model, but this would underestimate the inductive effect at low frequencies. Second, the attenuation suffered by the signal due to line resistance is underestimated. Finally, the higher inductance leads to a higher characteristic impedance and incorrectly predicts loss of matching at the input.

VI. CONCLUSIONS

We proposed a new methodology for skin effect equivalent circuits, based on the fitting of the transfer function to numerical simulations. It is shown that the methodology allows arbitrary accuracy in the modelling of the skin effect, and can be adapted to different situations and modelling requirements. We propose a method for the calculation for the skin effect of RLC interconnects. It is shown that skin effect can be computed efficiently in the s-domain using an algebraic formulation, instead of the improper integration in the time domain. The proposed method of computing skin effect relies on the poles and residues of the transfer function and can be used in any kind of model order reduction technique. Compact expressions that describe the skin effect on a single distributed RLC interconnect are rigorously derived. The derived expression along with the analysis can serve as a convenient tool for skin effect without much computation during design. In this paper, we have also proposed a novel analytical model to find the impact of the skin effect on the noise in RLC

interconnect without considering the skin effect on inductance because the value of the resistance increases dramatically with compare to the value of inductance. This paper also reflects that the crosstalk noise and delay increases rapidly in

comparison to the step input. Simulation results demonstrate the validity and correctness of our proposed model.

REFERENCES

[1] B. Kleveland, C. Diaz, D. Vook, L. Madden, T. Lee, and S. Wong, "Exploiting CMOS reverse interconnect scaling in multi-gigahertz amplifier and oscillator design," IEEE J. Solid-state Circuits, vol. 36, no. 10, pp. 1480–1488, Oct. 2001.

[2] M. Celik, L. Pileggi, A. Odabasioglu, "IC Interconnect Analysis" by Kluwer Academic Publishers, 2002.

[3] W. C. Elmore, 'The Transient Response of Damped Linear Networks with Particular Regard to Wideband Amplifiers", J. Applied Physics, vol. 19, no. 1, Jan. 1948. pp. :55 - 63

[4] Shien-Yang Wu, Boon-Khim Liew, K.L. Young, C.H. Yu, and S.C "Analysis of Interconnect Delay for 0.18µm Technology and Beyond" Interconnect Technology,. IEEE International Conference-1999 . Pages :68 – 70

[5] Magdy A. El-Moursy, Eby G. Friedman, "Optimum wire sizing of RLC interconnect with repeaters" INTEGRATION, the VLSI journal, 38 (2004) 205–225.

[6] Bhaskar Mukherjee, Lei Wang, Andrea Pacelli "A Practical Approach to Modeling Skin Effect in On-Chip Interconnects" Proceedings of the 14th ACM Great Lakes symposium on VLSI 2004.

[7] T.C.Edwards,M.B.Steer"Foundations of Interconnect and Microstrip Design",Third Edition,John Wiley & Sons.Ltd.

[8] B.K. Sen, R.L. Wheeler "Skin Effects models for Transmission Line Structures using Generic SPICE Circuit Simulators", IEEE 7th Topical meeting 26-28 Oct 1998, pp.128 – 131.

[9] Douglas Brooks Ultracad Design, Inc; article appeared in Printed Circuit Design and Manufacturing, UP Media, in December, 2009; http://www.ultracad.com.

[10] Rajib Kar, V. Maheshwari, Aman Choudhary, Abhishek Singh, "Coupling Aware Explicit Delay Metric for On-Chip RLC Interconnect for Ramp input", International Journal of Signal & Image Processing (IJSIP), Vol. 1, Issue 2, pp. 14-19, 2010, ACEEE, USA

[11] Madhumanti Datta, Susmita Sahoo, Debjit Ghosh, Rajib Kar, "An Accurate Analytical Crosstalk Model for On-Chip VLSI RLC Interconnect", International Journal of VLSI Design, International Sciences Press, vol 2 (1), pp. 83-89, 2011, India.

[12] Susmita Sahoo, Madhumanti Datta, Rajib Kar, "Delay and Power Estimation for CMOS Inverter Driving RLC Interconnect Loads", International Journal of Electrical and Electronics Engineering, Vol. 5, Issue. 3, pp. 165-172, WASET Publication, 2011, WASET Publication

[13] Susmita Sahoo, Madhumanti Datta, Rajib Kar, "Closed Form Solution for Delay and Power for a CMOS Inverter Driving RLC Interconnect under step Input" Journal of Electronic Devices, Vol. 10, 2011, pp. 464-470, France.

[14] Madhumanti Datta, Susmita Sahoo, Debjit Ghosh, Rajib Kar, "An Accurate Analytical Crosstalk Model for On-Chip VLSI RLC Interconnect", International Conference on Communication and Signal Processing (ICCOS'11), pp. 1133-1137, March 17-18, 2011, Coimbatore, India

[15] J. Zhang and E. G. Friedman. "Effect of Shield Insertion on Reducing Crosstalk Noise between Coupled Interconnects". Proceeding of the IEEE International Symposium on Circuit and Systems, Vol. 2, pp. 529-532, May 2004.

[16] Y. Massoud, J. Kawa, D. MacMillen, J. White. Modeling and Analysis of Differential Signaling for Minimizing Inductive Cross-Talk. IEEE/ACM DAC 2001, June 18-22, 2001, Las Vegas, Nevada, USA.

[17] P.V.Hunagund, A.B.Kalpana, "Analytical noise modeling for shielding to reduce crosstalk noise in on-chip interconnects", International Journal of Computer Science and Network Security, VOL.10 No.11,pp. 19-23, November 2010.

[18] Wigington, R.L.; Nahman, N.S.; "Transient Analysis of Coaxial Cables Considering Skin Effect," Proceedings of the IRE, vol.45, no.2, pp.166-174, Feb.1957.

[19] Reference Data for Radio Engineers, Fifth Edition, Howard W Sams and Co, 1968.

[20] Charlet, F.; Bermond, C.; Putot, S.; Le Carval, G.; Flechet, B.; "Extraction of (R,L,C,G) interconnect parameters in 2D transmission lines using fast and efficient numerical tools, International Conferece on Simulation of Semiconductor Processes and Devices (SISPAD) 2000 ,pp-87-89.